A CMOS-compatible High-speed Silicon Lateral Trench Photodetector

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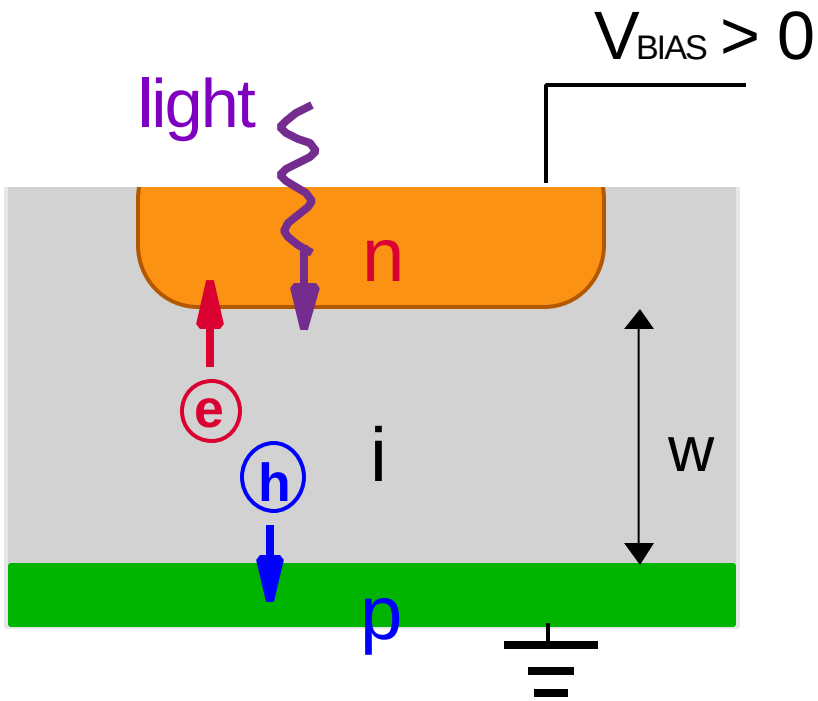
Limitations of Traditional Silicon p-i-n Photodiode

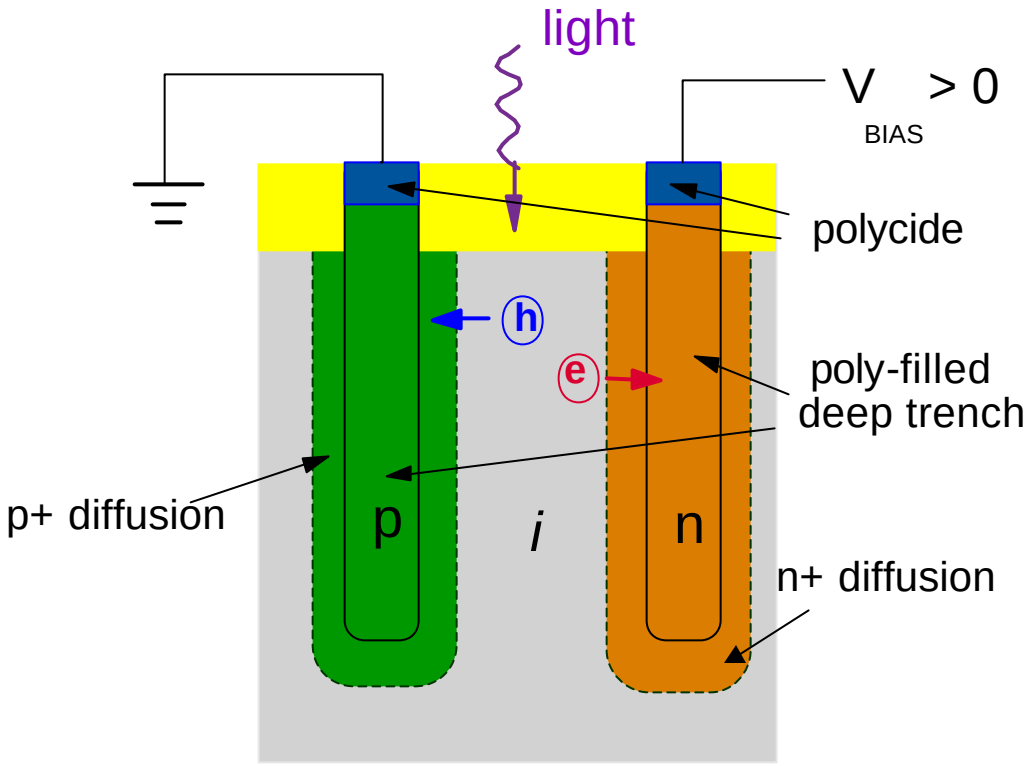


- Carrier transit time ~W^{-1}
- Light absorption ~$1-e^{-\alpha W}$

at 845nm
$\alpha^{-1} \approx 15\mu m$ in silicon

- There is a trade-off between speed and quantum efficiency for silicon p-*i*-n photodiode.
- Conventional (non-resonance enhanced) Si PIN (or MSM) external η<30% with 3-dB bandwidth >2GHz

Advantages of Lateral Trench Detector (LTD)



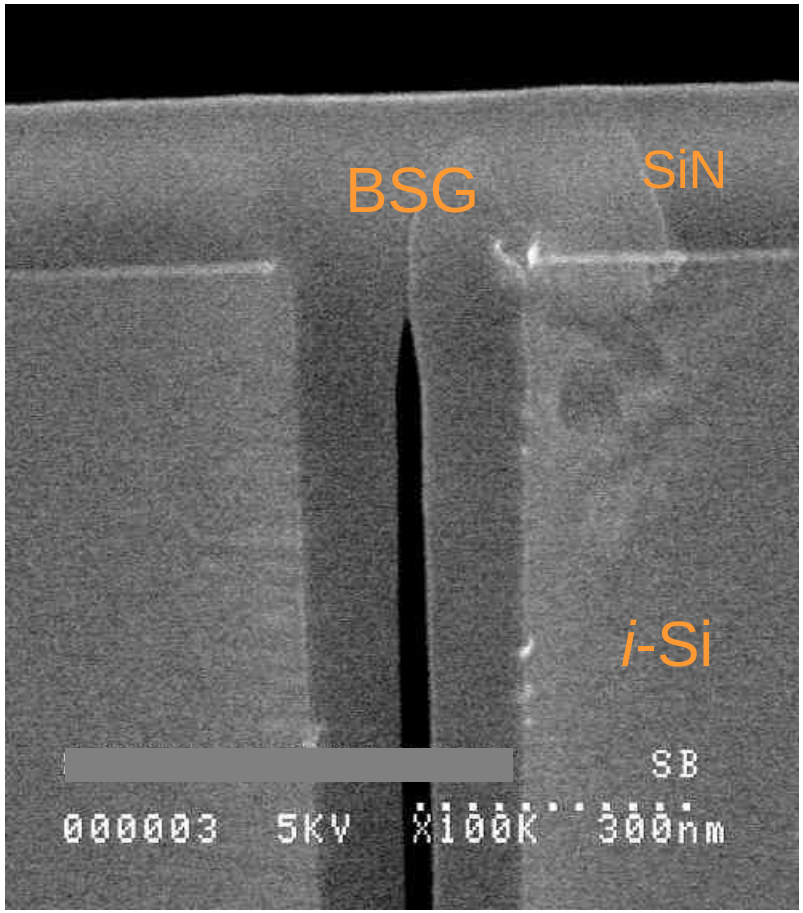
Main feature

- Deep trenches filled with p^+ or n^+ polysilicon
- Photo-generated carriers are collected laterally towards the trenches.

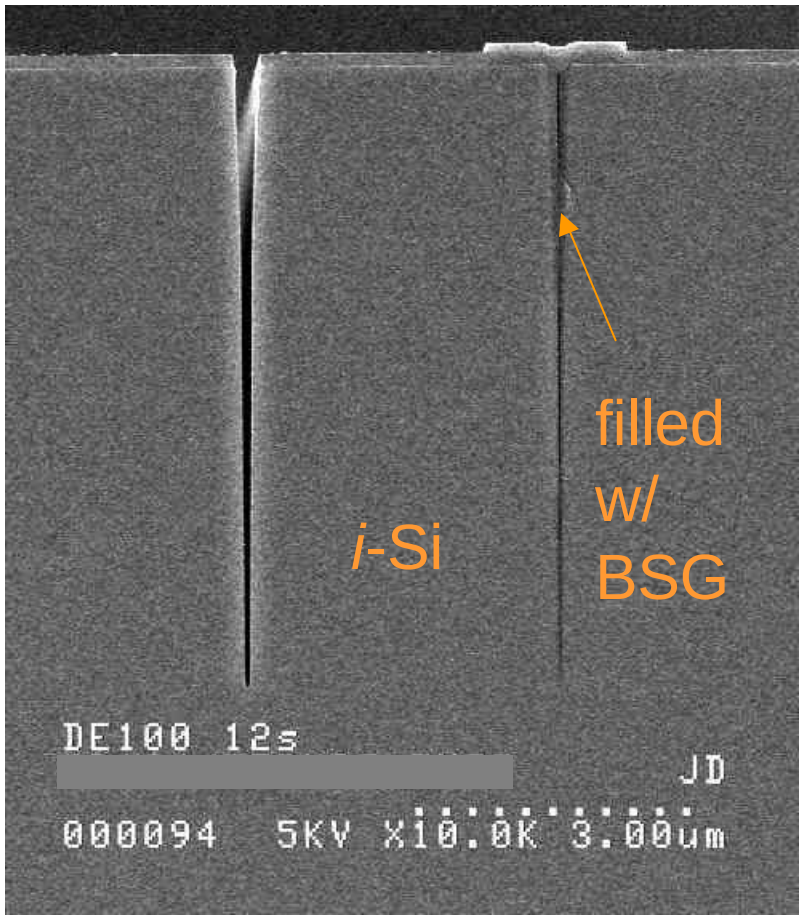
LTD decouples light absorption depth from the carriers transit distance ⇒ high speed and high quantum efficiency

Cross-sectional SEM of Lateral Trench Detector

After BSG CMP

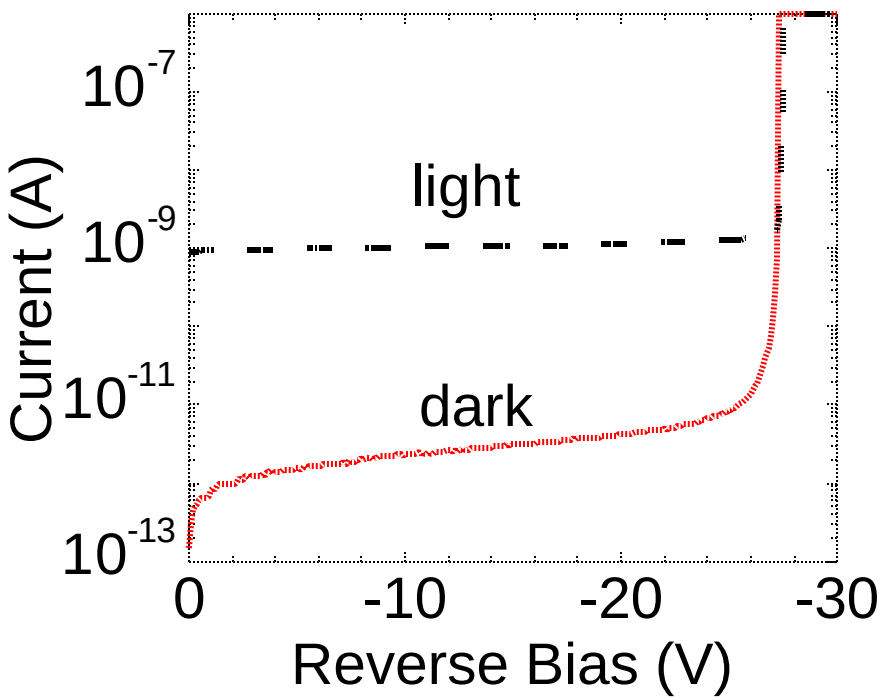


Before n^+ polysilicon deposition

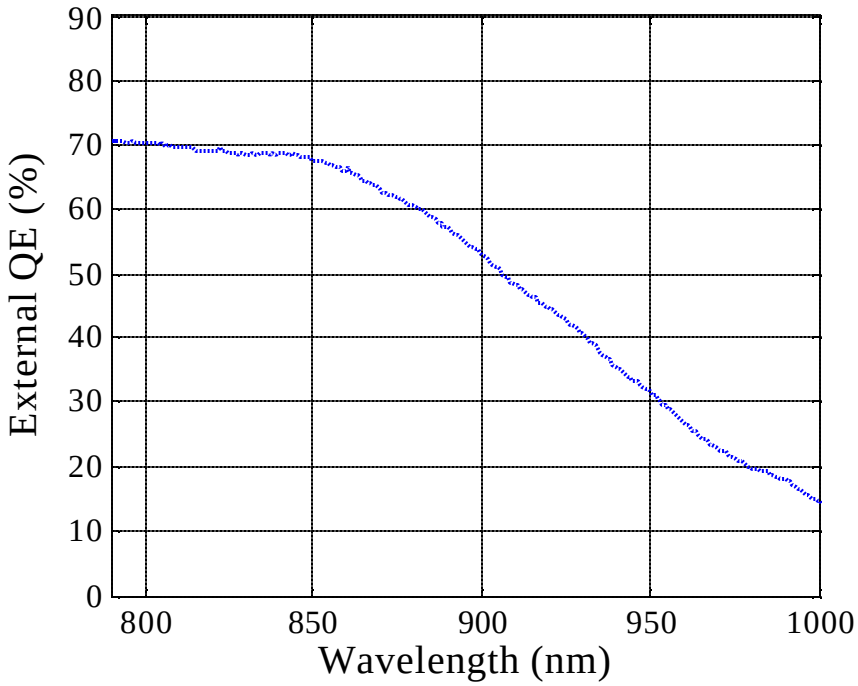


DC response from Lateral Trench Detector

Photo-current under white light/dark

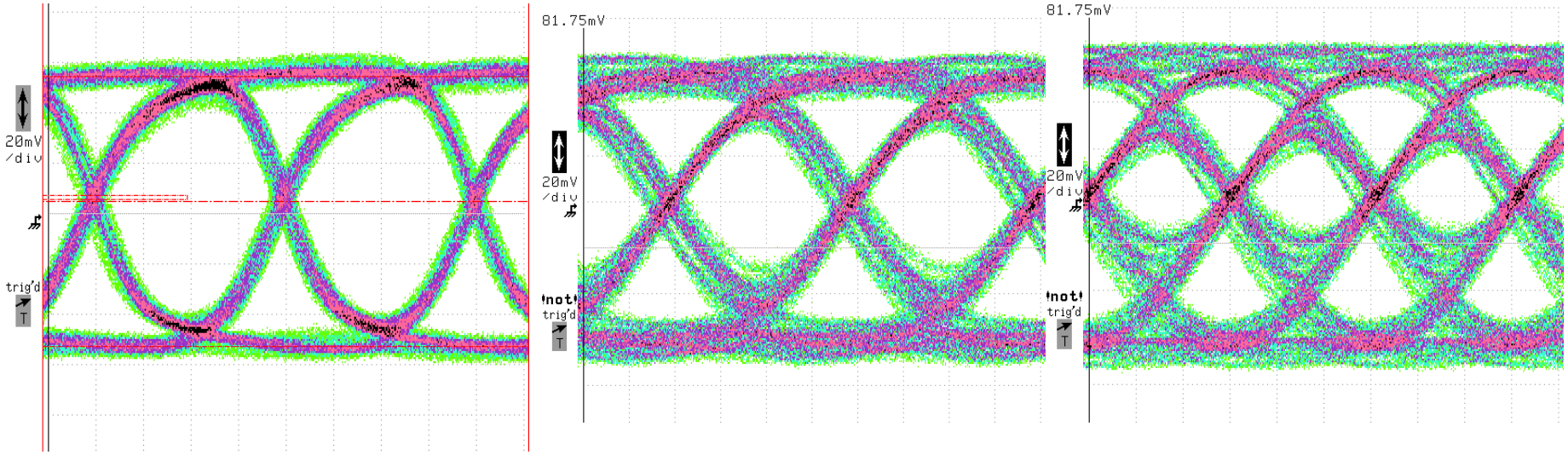


Quantum Efficiency vs. Wavelength



- Extremely low leakage current (~pA) and high breakdown voltage
- Response=0.45A/W at 845nm $\Rightarrow$ external quantum efficiency η=66% w/o anti-reflection coating

Eye-diagram of LTD wire-bond with BiCMOS TIA



2.5Gb/s **5.0Gb/s** **6.5Gb/s**

- 845nm wavelength laser was modulated at 2^7-1 PRBS data pattern
- Supply voltage is 3.3V